Design for testability in asynchronous digital controllers: an automated flow to design and validate asynchronous logic for digital controllers

life.augmented

By Francesco Battini, Enea Dimroci, Roberta Priolo, Marco Leo from STMicroelectronics
eMail: francesco.battini@st.com, enea.dimroci@st.com, roberta.priolo@st.com, marco.leo@st.com

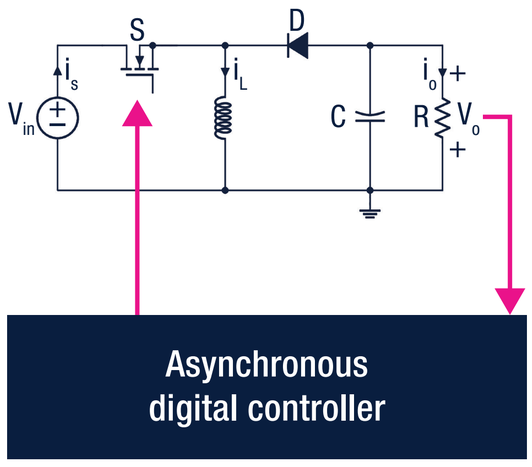
1. MOTIVATION

Complexity of power management IC and analog IPs designed with switched capacitor is increasing, and hence the complexity and the performances of their digital controllers.

Implementation of such digital controllers with asynchronous logic (usually state machines) is more suitable as they are more reactive, less area and power consuming and they don't require clock tree and fast clocks.

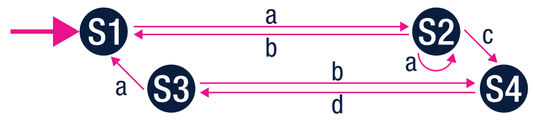
Automated test pattern generation (ATPG) with EDA tools currently is not able to reach high testability coverage for this kind of logic.

Solution: An automated flow has been developed, which is able to generate RTL and testability structure in order to detect stuck-at faults in asynchronous digital controllers.



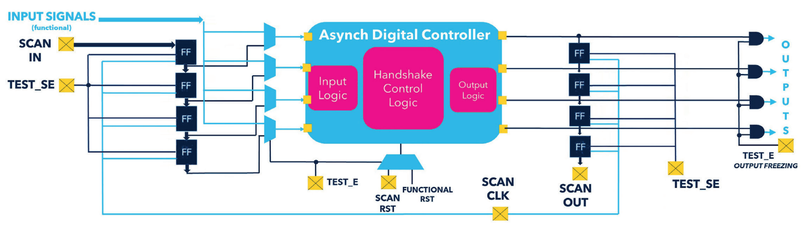
2. FLOW

Specifications — Text files (.gv and .csv files) describing the asynchronous state machine.



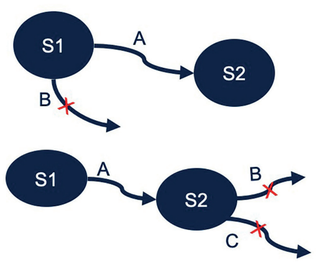
Hardware generator

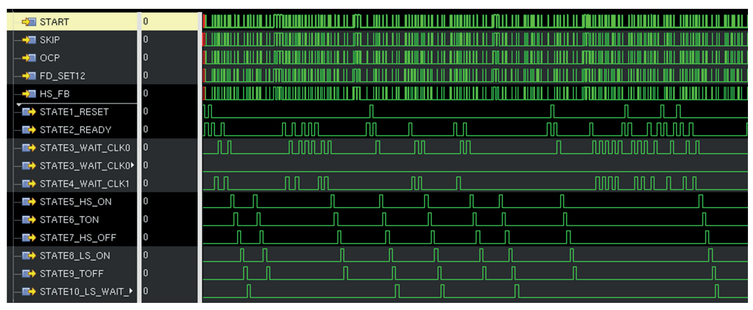
- RTL description of the asynchronous state machine.
- DFT architecture: flip flop scan architecture for detectability and observability.



Testbench generator

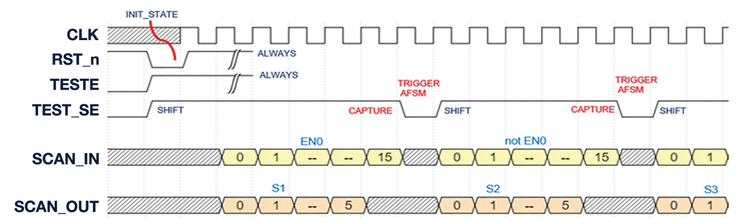
- An algorithm analyzes the flow chart and determines the minimum path that covers all the states and transitions of the controller.
- Testbench is automatically generated following the rules:
  - Trigger only one arc from current state
  - Inhibit transitions from destination state





Test pattern Generator (custom ATPG)

- Test patterns are generated using the output of the above algorithm, in order to minimize the number of test patterns and reduce test time.
- Test patterns are given to the product engineer to be used in ATE.



Fault coverage analysis

Given current architecture (number of states, arcs) and toggle coverage analysis the flow can calculate the expected stuck-at-fault coverage.

Toggle coverage + Architecture of controller → Fault Coverage %

RESULTS AND CONCLUSIONS

Demand for high-performance digital controllers for PMIC and switched capacitors devices is dramatically increasing

Asynchronous finite state machines are usually the best solution for a controller in such kinds of devices

Current EDA tools are not able to generate effective testability for these types of IPs

A fully automated flow has been developed.
It generates RTL with custom DFT architecture, testbenches, test patterns for ATE, and fault coverage analysis

ADVANTAGES

- Stuck-at-fault coverage up to 100 % (and always above 99%), with respect to ~30% of functional tests
- Drastic reduction of design time (up to 70%)
- This flow has been successfully applied in many products